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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,414	10/02/2003	Xinmin Tian	INTEL/17225	8460

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EXAMINER	
INGBERG, TODD D	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/677,414	TIAN ET AL.	
	Examiner	Art Unit	
	Todd Ingberg	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 5/5/2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) 1-15 is/are allowed.

6)☒ Claim(s) 16-34 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 October 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 1/04,2/06,5/06.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 34 have been examined.

Information Disclosure Statement

1. The Information Disclosure Statements filed May 5, 2006 and October 16, 2006 have been considered.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 16 – 34 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The current focus of the Patent Office in regard to statutory inventions under 35 U.S.C. § 101 for method claims and claims that recite a judicial exception (software) is that the claimed invention recite a practical application. Practical application can be provided by a physical transformation or a tangible result. No physical transformation is recited and additionally, the final result of the claim is a way to improve

latency memory in the runtime environment which is not a tangible result because the threads the inserted code is going into is not clearly and concisely claimed to be tangibly embodied on a computer readable medium. The following link on the World Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. §101.

<http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf>

Allowable Subject Matter

5. Claims 1 – 15 are allowed.

In reviewing the prior art of record under the standard of review as defined by the substantial evidence rules from Zurko V. Dickenson. The Examiner reviewed the X reference from the PCT application. "Speculative Pre computation Exploring the Use of Multithreading for Latency, Intel publication by Hong Wang et al. The claimed invention claims inserting two threads and a counting mechanism into the main thread. Page 5 teaches threads inserted into the main thread. However, the reference is silent as to the thread inserted into the main thread as containing the counting mechanism. The counter is identifies as being in the Outstanding Slice Counter (OSC).

All the claims are presented below.

Claim 1
A method of reducing memory latency in a software application, the method comprising:
analyzing the software application and determining a first area of software instructions that encounters a cache miss;
generating a helper thread;
generating a first set of compiler-runtime instructions and inserting the first set of compiler-runtime instructions in a main thread;
generating a second set of compiler-runtime instructions and inserting

the second set of compiler-runtime instructions in the helper thread; and

inserting a counting mechanism in the main thread and the helper thread, the counting mechanism being structured to coordinate relative execution points of the main thread and the helper thread.

Claim 2

A method as defined in claim 1, further comprising analyzing the software application and determining a second area of software instructions which encounters a memory load latency.

Claim 3

A method as defined in claim 2, wherein the first area of software instructions is different than the second area of software instructions.

Claim 4

A method as defined in claim 2, wherein the first area of software instructions comprises the second area of software instructions.

Claim 5

A method as defined in claim 2, wherein analyzing the software application comprises: measuring cache miss rates associated with the software application using a performance analysis tool; measuring memory load latencies associated with the software application using the performance analysis tool; reporting the first area of software instructions which encounters the cache miss to a compiler; and reporting the second area of software instructions which encounters the memory load latency.

Claim 6

A method as defined in claim 1, wherein generating a helper thread includes generating a thread graph.

Claim 7

A method as defined in claim 6, wherein the thread graph presents a data structure that represents a relationship between the main thread and the helper thread.

Claim 8

A method as defined in claim 6, wherein the thread graph facilitates code reuse.

Claim 9

A method as defined in claim 1, wherein at a least part of the first set of compiler-runtime instructions comprises at least a part of the second set of compiler-runtime instructions.

Claim 10

A method as defined in claim 1, wherein the first set of compiler runtime instructions inserted in the main thread comprises instructions to spawn the helper thread, terminate the helper thread, and coordinate execution of the helper thread and the main thread.

Claim 11
A method as defined in claim 1, wherein the second set of compiler runtime instructions inserted in the helper thread comprises instructions to coordinate execution of the helper thread and the main thread.

Claim 12
A method as defined in claim 1, wherein the counting mechanism comprises a software counter.

Claim 13
A method as defined in claim 12, wherein at least one of the first set of compiler-runtime instructions and the second set of compiler-runtime instructions include instructions to control execution rates of the helper thread based on a value associated with the software counter.

Claim 14
A method as defined in claim 12, wherein at least one of the first set of compiler-runtime instructions and the second set of compiler-runtime instructions include instructions to control execution rates of the main thread based on a value associated with the software counter.

Claim 15
A method as defined in claim 14, wherein the compiler-runtime instructions to control execution rates comprises a delay instruction, a catch up instruction and an instruction to force execution.

Claim 16
A system to reduce memory latency, the system comprising:
a processor;
a memory operatively coupled to the processor:
the memory storing a software tool structured to identify a code region in an application program that suffers from a data cache miss;
a compiler operatively coupled to the software tool, the compiler being structured to receive information from the software tool and to generate a helper
a set of compiler-runtime instructions to be generated and inserted in the application program to manage the helper thread and to manage a main thread; and a counting mechanism for insertion in the main thread and the helper thread to facilitate coordination of execution points associated with the helper thread and the main thread.

Claim 17
A system as defined in claim 16, wherein the software tool comprises a Tune Performance Anaylyzer.

Claim 18

A system as defined in claim 16, wherein the information the compiler receives from the software tool comprises data cache miss rates associated with the identified code region.

Claim 19
A system as defined in claim 16, wherein the information the compiler receives from the software tool comprises memory load latency times associated with the identified code region.

Claim 20
A system as defined in claim 16, wherein the helper thread is structured to prefetch variables contained in the identified code region.

Claim 21
A system as defined in claim 16, wherein the set of compiler-runtime instructions comprises instructions to create the helper thread, terminate the helper thread, delay execution of the helper thread, and activate the helper thread.

Claim 22
A system as defined in claim 16, wherein the set of compiler-runtime instructions comprises instructions to coordinate execution of the helper thread and the main thread.

Claim 23
A machine readable medium storing instructions to cause a machine to: analyze a software application including a main thread; identify a code region in the software application; generate a helper thread; generate and insert a first set of compiler-runtime instructions in the main thread to manage the helper thread and the main thread; generate and insert a second set of compiler-runtime instructions in the helper thread to manage the helper thread and the main thread; and manage execution points of the helper thread and the main thread.

Claim 24
A machine readable medium as defined in claim 22, wherein the stored instructions are structured to cause the machine to identify the code region based on cache miss rates.

Claim 25
A machine readable medium as defined in claim 22, wherein the stored instructions are structured to cause the machine to identify the code region based on memory load latencies.

Claim 26
A machine readable medium as defined in claim 22, wherein the stored instructions are structured to cause the machine to generate the helper thread to prefetch instructions within the identified code region.

Claim 27

A machine readable medium as defined in claim 22, wherein the stored instructions are structured to cause the machine to generate compiler-runtime instructions to spawn the helper thread, terminate the helper thread, coordinate execution of the helper thread and the main thread.

Claim 28
A machine readable medium as defined in claim 22, wherein the stored instructions are structured to cause the machine to manage the execution of the main thread and the helper thread by inserting a first portion of a counting mechanism in the main thread and a second portion of a counting mechanism in the helper thread.

Claim 29
An apparatus to reduce memory latency, the apparatus comprising: a software tool structured to identify a code region in an application program that suffers from a data cache miss; a compiler operatively coupled to the software tool, the compiler being structured to receive information from the software tool and to generate a helper thread; a set of compiler-runtime instructions to be generated and inserted in the application program to manage the helper thread and to manage a main thread; and a counting mechanism for insertion in the main thread and the helper thread to facilitate coordination of execution points associated with the helper thread and the main thread.

Claim 30
An apparatus as defined in claim 29, wherein the information the compiler receives from the software tool comprises data cache miss rates associated with the identified code region.

Claim 31
An apparatus as defined in claim 29, wherein the information the compiler receives from the software tool comprises memory load latency times associated with the identified code region.

Claim 32
An apparatus as defined in claim 29, wherein the helper thread is structured to prefetch variables contained in the identified code region.

Claim 33
An apparatus as defined in claim 29, wherein the set of compiler runtime instructions comprises instructions to create the helper thread, terminate the helper thread, delay execution of the helper thread, and activate the helper thread.

Claim 34
An apparatus as defined in claim 29, wherein the set of compiler runtime instructions comprises instructions to coordinate execution of the helper thread and the main thread.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Todd Ingberg whose telephone number is (571) 272-3723. The examiner can normally be reached on during the work week..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Todd Ingberg
Primary Examiner
Art Unit 2193

TI